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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,185	02/01/2002	Koji Shimbayashi	024016-00025	9530

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,185	SHIMBAYASHI ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,28-37,40-42,44,46 and 47* is/are rejected.

7)☒ Claim(s) *21–27, 38, 39, 43 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 01, 2002.

2. Claims 1 – 47 are pending in this case. Claims 1, 8, 20, 29, 41, and 44 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1–20, 28–37, 40–42, 44, 46 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Tedrow et al. U.S. Patent No. 6,515,906 – filed Dec. 28, 2000.

Regarding independent claim 1, Fig. 5 of Tedrow et al. discloses a nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) including a plurality of digit lines (Odd and Event Global bit lines) to which a plurality of nonvolatile memory cells are connected (Block 0 – Block 7), wherein upon reading of memory cell information (Col. 5 lines 62 – 67), the digit lines contain a first digit line (Odd Global Bit line) connected to selected one of the nonvolatile memory cells (Block 7, Block 1); and a second digit line

(Even Global Bit Line) connected to only non-selected nonvolatile memory cells (Block 6, Block 0), while the memory cell information is read out with the first and second digit lines as a pair (Drain Bias & Sense Amplifier).

Regarding dependent claim 2, Tedrow discloses wherein the first digit line and the second digit line adjoin each other (Drain Bias & Sense Amplifier).

Regarding dependent claim 3, Tedrow discloses wherein the first digit line and the second digit line have equivalent physical parameters surrounding the first and second digit lines (Blocks, Global Y Selects, Reference Cell Array, Amplifier).

Regarding dependent claim 4, Fig. 5 of Tedrow et al. further comprising a plurality of sectors (Global Y Selects), each of the sectors including a predetermined number ([Block 0, Block 6]; [Block 1, Block 7]) of the nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein a positional relationship of the first digit line and the second digit line is inverted by each of the sector (Col. 6 lines 35 – 40).

Regarding dependent claim 5, Fig. 5 of Tedrow et al. further comprising a plurality of sectors (Global Y Selects), each of the sectors including a predetermined number of the nonvolatile memory cells ([Block 0, Block 6]; [Block 1, Block 7]) and serving as a basic unit for accessing the nonvolatile memory cell, wherein the first digit line is disposed in a first sector while the second digit line is disposed in a second sector (Drain Bias & Sense Amplifier).

Regarding dependent claim 6, Tedrow discloses wherein the first sector and the second sector are disposed adjoining each other (Drain Bias & Sense Amplifier + -).

Regarding dependent claim 7, Tedrow discloses wherein the first digit line and the second digit line have equivalent physical parameters surrounding the digit line (Reference Array, Global Y Selects, Sense amplifier, Memory Blocks).

Regarding independent claim 8, Fig. 7 of Tedrow et al. discloses a nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) having a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected (715A – 745A, 715B - 745B) and a global digit line (ODD, EVEN Global Bit Lines) provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected (715 – 745), wherein upon reading memory cell information (Col. 5 lines 62 – 67), the global digit lines include: a first global digit line (ODD Global Bit Line) connected to a first local digit line (715B – 745B) to which the selected nonvolatile memory cell is connected; and a second global digit line (EVEN Global Bit Line) adjacent the first global digit line, to which the selected nonvolatile memory cell is not connected (715A – 745A), while the memory cell information is read out with the first and second global digit lines as a pair (Fig. 5 [Sense Amplifier]).

Regarding dependent claim 9, Tedrow discloses wherein the second global digit line (Even Global Bit Line) is connected to a second local digit line (715A – 745A) to which only the non-selected nonvolatile memory cells are connected.

Regarding dependent claim 10, Tedrow discloses wherein the first local digit line and the second local digit line adjoin each other (Fig. 2 (Drain Bias & Sense Amplifier + -)).

Regarding dependent claim 11, Tedrow discloses wherein the first local digit line and the second local digit line have equivalent physical parameters surrounding the first and second local digit lines (Figs. 2 and 7).

Regarding dependent claim 12, Fig. 6 of Tedrow further comprising a plurality of sectors (Odd Block, Even Block), each of the sectors including a predetermined number of the nonvolatile memory cells (715 – 745) and serving as a basic unit for accessing the nonvolatile memory cell, wherein a positional relationship of the first local digit line and the second local digit line is inverted every sector (Col. 6 lines 35 – 40).

Regarding dependent claim 13, Fig. 7 of Tedrow et al. further comprising a plurality of sectors (Even Block, Odd Block), each of the sectors including a predetermined number (715 – 745) of the nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein the first local digit line is disposed in a first sector while the second local digit line is disposed in a second sector (Fig. 5 (Drain Bias & Sense Amplifier)).

Regarding dependent claim 14, Tedrow discloses wherein the first sector and the second sector are disposed adjoining each other (Fig. 5 (Drain Bias & Sense Amplifier)).

Regarding dependent claim 15, Tedrow discloses wherein the first local digit line and the second local digit line have equivalent physical parameters surrounding the local digit line (Fig. 5, 6 and 7).

Regarding dependent claim 16, Tedrow discloses wherein the positional relationship of the first global digit line and the second global digit line is inverted by each of the sector (Col. 6 lines 35 – 40).

Regarding dependent claim 17, Tedrow discloses wherein a positional relationship of the first global digit line and the second global digit line is inverted every sector (Fig. 5 [Block 0, Block 1, Block 6, Block 7).

Regarding dependent claim 18, Tedrow discloses wherein a minimum unit of redundant configuration for recovery of a defect comprised the first (ODD Bit Lines) and second (EVEN Bit Lines) digit lines making a pair (Sense Amplifier). Although Tedrow et al. is silent to wherein a minimum unit of redundant configuration for recovery of a defect, however the recitation a minimum unit of redundant configuration for recovery of a defect has not been given patentable weight because it has been held that a preample is denied the effect of a limitation where the claim is draw to a structure and portion of the claim following the preample is a self-contained description of the structure not depending for completeness upon introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

Regarding dependent claim 19, Tedrow discloses wherein a minimum unit of redundant configuration for recovery of a defect comprised the first (ODD Bit Lines) and second (EVEN Bit Lines) digit lines making a pair (Sense Amplifier). Although Tedrow et al. is silent to wherein a minimum unit of redundant configuration for recovery of a defect, however the recitation a minimum unit of redundant configuration for recovery of a defect has not been given patentable weight because it has been held that a

preample is denied the effect of a limitation where the claim is draw to a structure and portion of the claim following the preample is a self-contained description of the structure not depending for completeness upon introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

Regarding independent claim 20, Fig. 7 of Tedrow et al. discloses a nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) including a plurality of digit lines (Odd and Event Global bit lines) to which a plurality of nonvolatile memory cells are connected (Odd, Even Blocks), wherein the digit lines include a first digit line (Odd Global Bit Line) to which a selected one of the nonvolatile memory cells (Odd Block) is connected; and a second digit line (Even Block) to which only non-selected nonvolatile memory cells are connected, the nonvolatile semiconductor memory device further comprising a selecting portion provided (Fig. 5 [Global Y Selects) for every predetermined number of the digit lines and for, upon reading memory cell information, selecting both the first and second digit lines and (Col.5 lines 62 – 67), upon writing memory cell information, selecting only the first digit line (this is inherent to structures of Fig. 5, because upon storing or writing information to an odd memory cell, only odd global bit line is needed to be select by the Global Y Selects to have data from the Odd Global bit line storing to selected memory cell) .

Regarding dependent claim 28, Fig. 7A of Tedrow et al. further comprising a plurality of local digit lines (715 - 745) to which a plurality of nonvolatile memory cells are connected and a global digit line (Odd, Even Global bit Lines) provided for each

predetermined number of the local digit lines and to which the local digit line is selectively connected, wherein the digit line is the global digit line (Fig. 7A).

Regarding independent claim 29, Fig. 7 of Tedrow et al. discloses a nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) including a plurality of digit lines (715 - 745) to which a plurality of nonvolatile memory cells are connected and a data line (Odd Global Bit Line) connected selectively (717 – 747) to the digit line, the nonvolatile semiconductor memory device further comprising: a first data line (ODD Global Bit Line) to which the selected nonvolatile memory cell is connected through a first digit line (715b – 745B); a second data line (Even Global Bit Line) to which only the non-selected nonvolatile memory cells are connected through a second digit line (715A – 745A); a first loading portion (Fig. 5 Odd Global Y Selects) connected to the first data line (Odd Global Bit Line); and a second loading portion (Fig. 5 Even Global Y Selects) having a structure equivalent to that of the first loading portion, connected to the second data line (Even Global Bit Line) and for supplying a reference current (Fig. 5 Reference Cell Array) to a current flowing through the first data line based on the memory cell information (Col. 3 lines 61 – 64, also see Fig. 6), wherein the memory cell information is read out with the first and second data lines as a pair (Col. 5 lines 62 – 67).

Regarding dependent claim 30, Tedrow discloses wherein the first and second loading portions have a load equivalent (Fig. 5 Reference Cell Array) to a load (Fig. 5 Blocks) existing on a path leading from the nonvolatile memory cell to the first and second loading portions (Fig. 5).

Regarding dependent claim 31, Tedrow discloses wherein the first and second loading portions have first and second reference cells equivalent to the nonvolatile memory cell (Fig. 5 [Reference Cell Array] X's crossed).

Regarding dependent claim 32, Fig. 6 of Tedrow et al. further comprising a regulating portion containing a third reference cell (610) equivalent to the nonvolatile memory cell, for generating a reference current with respect to a current based on the memory cell information and outputting a regulation voltage corresponding to the reference current (Col. 7 lines 1 – 21), wherein the first and second loading portions (Fig. 5 (Global Y Selects Transistors) have first and second load portions (Fig. 6 [630, 620]) in which a current value is controlled by the regulation voltage (Col. 7 lines 1 – 21).

Regarding dependent claim 33, Tedrow discloses wherein the first and second reference cells (Fig. 5 X's crossed of Reference Cell Array) are disposed in a region (Fig. 5 Reference Cell Array Block) different from an arrangement region of the nonvolatile memory cell in which the memory cell information is stored (Block 0 – Block 7).

Regarding dependent claim 34, Fig. 6 of Tedrow et al. further comprising first and second selecting switches (630, 620) for connecting the first and second reference cells to a reference potential, wherein any one of the first selecting switch and the second selecting switch is selectively turned on (Col. 6 lines 56 – 67).

Regarding dependent claim 35, Tedrow discloses wherein the third reference cell (Fig. 6 [610]) is disposed in a region (Fig. 5 Reference Cell Array Blocks) different

from an arrangement region of the nonvolatile memory cell in which the memory cell information is stored (Fig. 5 Memory Blocks 1 – 7).

Regarding dependent claim 36, Fig. 6 of Tedrow et al. further comprising first and second selecting switches (630, 620) for connecting the first and second reference cells to a reference potential (Col. 7 lines 1 – 21), wherein any one of the first selecting switch and the second selecting switch is selectively turned on (Col. 6 lines 56 – 67).

Regarding dependent claim 37, in Fig. 6 of Tedrow et al. further discloses wherein the regulating portion includes a reference current generating portion containing the third reference cell (610), and a regulation voltage generating portion (Fig. 6) containing a third load portion (630, 620) equivalent to the first and second load portions (Fig. 5 Global Y Selects transistors).

Regarding dependent claim 40, Fig. 7 of Tedrow et al. further comprising a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected (715 – 745) and a global digit line (Odd and Even Global bit lines) provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected (717 – 747), wherein the digit line is the global digit line.

Regarding independent claim 41, Fig. 5 of Tedrow et al. discloses nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) having a plurality of digit lines (Odd and Event Global bit lines) to which a plurality of nonvolatile memory cells are connected (Block 0 – Block 7) and a data line connected (Fig. 7 [715 – 745]) selectively (Fig. 7 [717 – 747]) to the digit line, the nonvolatile semiconductor memory device further comprising: a first data line (Fig. 7 [715B – 745B]) to which the selected

nonvolatile memory cell is connected through the digit line and through which a current based on memory cell information flows; a second data line (Fig. 7 [715 A – 745A]) through which a reference current flows; and a current comparing portion (Fig. 5 [Drain Bias & Sense Amplifier]) to which the first and second data lines are connected and which compares a current based on the memory cell information with the reference current (Col. 3 lines 61 – 64), wherein the current comparing portion includes a current load portion having a current mirror structure (+ non-inverted input, - inverted input of Drain Bias & Sense Amplifier in Fig. 5) and a connection changing portion (Fig. 5 [Y Global Selects]) for changing a connection between the first and second data lines and the current load portion.

Regarding dependent claim 42, Tedrow discloses wherein the connection changing portion is so controlled that the second data line is connected to a reference side (Fig. 6, Col. 6 lines 56 – 66) in the current mirror structure of the current load portion (+ non-inverted input, - inverted input of Drain Bias & Sense Amplifier in Fig. 5).

Regarding independent claim 44, Fig. 5 of Tedrow et al. discloses nonvolatile semiconductor memory device (Col. 4 lines 55 – 57) having a plurality of digit lines (Odd and Event Global bit lines) to which a plurality of nonvolatile memory cells are connected (Block 0 – Block 7) and a data line connected (Fig. 7 [715 – 745]) selectively (Fig. 7 [717 – 747]) to the digit line, the nonvolatile semiconductor memory device further comprising: a first data line (Fig. 7 [715B – 745B]) and through which a current based on memory cell information flows; a second data line (Fig. 7 [715 A – 745A]) through which a reference current flows; and a current comparing portion (Fig. 5 [Drain

Bias & Sense Amplifier]) to which the first and second data lines are connected and which compares a current based on the memory cell information with the reference current (Col. 3 lines 61 – 64), wherein the current comparing portion includes a current load portion (Fig. 6) for supplying a current equivalent (Fig. 6 [610]) to the reference current to the first and second data lines.

Regarding dependent claim 46, Fig. 6 of Tedrow et al., further comprising a bias portion for restricting a voltage applied to the first and second data lines side irrespective of a voltage outputted from the current load portion (Col. 7 lines 1 – 21).

Regarding dependent claim 47, Fig. 7 of Tedrow et al. further comprising a plurality of local digit lines (715 – 745) to which a plurality of nonvolatile memory cells are connected and a global digit line (Odd, Even Global Bit Lines) provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected (717 – 747), wherein the digit line is the global digit line.

Allowable Subject Matter

4. Claims 21–27, 38, 39, 43 and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

With Respect to claim 21, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "upon reading memory cell

information, connecting the digit line to the data line by a first current driving power and, upon writing memory cell information, connecting the digit line to the data line by a second current driving power, which is larger than the first current driving power".

With respect to claim 38, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the regulating portion includes a current mirror portion for mirroring a reference current generated by the reference current generating portion to the regulation voltage generating portion, and a feedback portion for controlling the third load portion so as to supply the mirrored reference current to the regulation voltage generating portion".

With respect to claim 43, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the connection changing portion includes a voltage dividing portion for restricting a voltage applied to the current load portion side irrespective of a voltage of the first and second data lines".

With respect to claim 45, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "a voltage dividing portion for restricting a voltage applied to the current load portion side irrespective of a voltage of the first and second data lines, the voltage dividing portion being provided between the first and second data lines and the current load portion".

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hidaka	Patent No. US 6,359,805 B1	Date of Patent: Mar. 19, 2002
Mochida	Patent No. US 6,091,662	Date of Patent: Jul. 18, 2000
Tsao et al.	Pub. No. US 2003/0039142 A1	Pub. Date: Feb. 27, 2003

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 8/4/2004

9/2/04

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800